WHAT IS CLAIMED IS:

1. A method of designing a semiconductor circuit having clock trees, the method comprising the steps of:

generating a netlist;

inserting a plurality of delay gates onto said netlist;

place;

generating ~~said~~ clock trees which satisfy a constraint of timing in said clock ~~tree~~ trees;

route;

manually adjusting skew between said clock trees by deleting some of said ~~inserted~~ inserted delay gates based on the constraint of ~~the~~ timing between said clock trees;

examining the skew between said clock trees;

determining whether ~~the~~ constraint of the timing is satisfied ~~or not~~; and

making a minimum change in ~~the~~ place and route in association with ~~the~~ insertion of said delay gates.

2. The method of designing a semiconductor circuit according to claim 1, wherein in the step of place, a plurality of delay gates on said clock line are collectively placed.

3. The method of designing a semiconductor circuit according to claim 1, wherein in the step of place, a plurality of delay gates on said clock line are collectively placed and a large region

is assured.

4. The method of designing a semiconductor circuit according to claim 2, wherein in ~~the step of~~ manually adjusting a skew between trees, said delay gates at ~~the~~ first and last stages among said ~~inserted~~ inserted delay gates are not ~~regarded as~~ targets to be deleted.

5. The method of designing a semiconductor circuit according to claim 3, wherein in ~~the step of~~ manually adjusting a skew between trees, said delay gates at ~~the~~ first and last stages among said ~~inserted~~ inserted delay gates are not ~~regarded as~~ targets to be deleted.

6. A semiconductor circuit having clock trees, said semiconductor circuit being designed using a designing method comprising the steps of:

generating a netlist;

inserting a plurality of delay gates onto said netlist;

place;

generating ~~said~~ clock trees which satisfy a constraint of timing in said clock ~~tree~~ trees;

route;

manually adjusting a skew between said clock trees by deleting some of said ~~inserted~~ inserted delay gates based on the constraint of ~~the~~ timing between said clock trees;

examining the skew between said clock trees;

determining whether ~~the~~ constraint of the timing is satisfied ~~or not~~; and

making a minimum change in ~~the~~ place and route in association with ~~the~~ insertion of said delay gates.